IN THE CLAIMS

For the Examiner's convenience, a list of all claims is included below.

What is claimed:

1. (Currently Amended) In a controller of a computing device, computing device comprising a system memory and a codec, a method comprising:

reading data from a buffer of the system memory via a first interface of the controller,

transferring the data to the codec via a second interface of the controller,

tracking a position in the buffer from which the controller has read the data, and

writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate the position in the buffer.

2. (Previously Presented) The method of claim 1 wherein the reading comprises isochronously receiving the data via the first interface.

3. (Original) The method of claim 1 further comprising tracking progress of transferring the data to the codec via the second interface.

4. (Original) The method of claim 1 wherein reading the data from the buffer comprises reading the data per a buffer descriptor list that defines the buffer.

5. (Previously Presented) The method of claim 4, wherein reading the data from the buffer further comprises returning to a start of the buffer in response to reaching an end of the buffer.

6. (Currently Amended) The method of claim 1 further comprises, prior to writing the value to system memory, determining whether to update the value in the system memory based upon the data transferred via the second interface.

7. (Currently Amended) In a controller of a computing device, the computing device comprising a system memory and a codec, a method comprising:

receiving data from the codec via a first interface of the controller,

writing the data to a buffer of the system memory via a second interface of the controller,

tracking a position in the buffer to which the controller has written the data, and

writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory via the second interface to indicate the position in the buffer.

8. (Original) The method of claim 7 wherein writing the data to the buffer comprises isochronously transferring the data toward the buffer via the second interface.

9. (Original) The method of claim 7 further comprising tracking progress of receiving the data from the codec via the first interface.

10. (Original) The method of claim 7 wherein writing the data to the buffer comprises writing the data per a buffer descriptor list that defines the buffer.

11. (Original) The method of claim 10 wherein writing the data to the buffer further comprises returning to a start of the buffer in response to reaching an end of the buffer.

12. (Original) The method of claim 7 further comprises determining, prior to writing the value to system memory, to update the value in the system memory based upon the data received via the first interface.

13. (Currently Amended) A system comprising

a processor,

a system memory comprising a buffer and a direct memory access position-in-buffer ~~position~~(DPIB) structure that indicates a position in the buffer,

an audio controller coupled to the system memory via a first bus, and

a codec coupled the audio controller via a second bus, wherein

the audio controller transfers data between the buffer and the codec via the first bus and the second bus and updates the buffer position via the first bus to indicate a the position in the buffer associated with the audio controller transferring between the buffer and the audio controller.

14. (Original) The system of claim 13 wherein the audio controller transfers the data across the first bus via an isochronous channel and updates the buffer position via the isochronous channel.

15. (Original) The system of claim 13 wherein the audio controller transfers the data across a link of the first bus and updates a link position counter of the audio controller based upon the data transferred across the link.

16. (Original) The system of claim 13 wherein the system memory further comprises a buffer descriptor list that defines the buffer and the audio controller transfers the data based upon the buffer descriptor list.

17. (Original) The system of claim 13 wherein the audio controller isochronously reads the data from the buffer via the first bus and transfers the data to the codec via the second bus.

18. (Original) The system of claim 13 wherein the audio controller receives the data from the codec via the second bus and isochronously writes the data to the buffer via the first bus.

19. (Currently Amended) A controller comprising

a first direct memory access controller to transfer data between a system memory and a codec via a first interface to the system memory and a second interface to the codec, and

a position controller to update a position value in a direct memory access position-in-buffer (DPIB) structure located in the system memory via the first interface to indicate progress of the first direct memory access controller in transferring data between the system memory and the codec.

20. (Original) The controller of claim 19 further comprising a second direct memory access controller

to read from the system memory a buffer descriptor list that defines a buffer in the system memory, and

to configure the first direct memory access controller to transfer the data between the buffer and the codec per the buffer descriptor list.

21. (Original) The controller of claim 19 further comprising a link counter to maintain a count indicating progress of the first direct memory access controller in transferring the data across the second interface.

22. (Original) The controller of claim 19 further comprising a buffer position counter to maintain a count indicating progress of the first direct memory access controller in transferring the data across the first interface.

23. (Original) The controller of claim 19 wherein the first direct memory access controller isochronously writes the data to the buffer.

24. (Original) The controller of claim 19 wherein the first direct memory access controller isochronously reads the data from the buffer.

25. (Currently Amended) A machine-readable medium comprising a plurality of instructions that in response to being executed result in a computing device

configuring an audio controller to stream data between a buffer in a system memory of the computing device and a codec of the computing device,

configuring the audio controller to update a buffer position indicative of progress of transferring data between the buffer and the codec in the system memory based upon progress of transferring data between the buffer and the codec, wherein the updating includes writing a value to a direct memory access position-in-buffer (DPIB) structure located in the system memory, and

reading the buffer position from the system memory to determine progress of the audio controller in streaming the data between the buffer and the audio controller.

26. (Original) The machine-readable medium of claim 25 wherein the plurality of instructions in response to being executed further result in the computing device

reading a link position from the audio controller to determine progress of the audio controller in streaming the data between the codec and the audio controller.

27. (Original) The machine-readable medium of claim 25 wherein the plurality of instructions in response to being executed further result in the computing device

allocating the buffer in the system memory and storing a buffer descriptor list in the system memory, and

configuring the audio controller to transfer the data per the buffer descriptor list.

28. (Original) The machine-readable medium of claim 25 wherein the plurality of instructions in response to being executed further result in the computing device

allocating a position in buffer structure in the system memory, and

configuring to update the position in buffer structure with the buffer position.